<u>In the claims:</u>

1. (currently amended) A communications switch for switching data between inputs and outputs, said communications switch comprising:

p inputs each for receiving data to be switched to q outputs;

p+k information storage buffers each of said information storage buffers comprising p+k storage locations;

an input data conditioner, comprising p inputs and p+k outputs, connected between said p inputs of said communications switch and said p+k information buffers, for distributing data received at said p inputs of said input data conditioner to its p+k outputs;

an ingress commutator for interconnecting each of said p+k information storage buffers to one of said p+k outputs of said input data conditioner;

an output data conditioner comprising p+k inputs and q outputs, for distributing data from its p+k inputs to its q outputs;

an egress commutator for interconnecting each of said p+k information storage buffers to one of said p+k inputs of said output conditioner;

said ingress commutator operable to cyclically interconnect each of said p+k outputs of said input data conditioner to each of said p+k information buffers to provide data from said each of said p+k outputs of said input data conditioner to said p+k information storage buffers, said egress commutator operable to cyclically interconnect each of said p+k information storage buffers to said p+k inputs of said output data conditioner to provide data from said p inputs to said q outputs;

<u>wherein p, q, and k are positive integers</u>.

2. (Original) The switch of claim 1, where p=q.

3. (Original) The switch of claim 1, wherein said ingress commutator is clocked at a rate to transfer less data to each of said p+k information storage buffers during a time interval than is received at each of said p inputs during said time interval.

4. (Original) The switch of claim 1, wherein said ingress commutator is clocked at a rate of 1/t to transfer data to each of said information buffers arriving at said input at a rate of 1/t' where t' = t*p/(p+k).

5. (Original) The switch of claim 1, wherein said input data conditioner comprises 2p(p+k) buffers for storing data received at said p inputs of said data conditioner.

6. (Original) The switch of claim 5, wherein said input data conditioner comprises p, (1 input, 2(p+k) output) data distributors each to present data at one of said inputs of said input data conditioner to one of said buffers.

7. (Original) The switch of claim 6, wherein said input data conditioner comprises p, 2(p+k) input data selectors, each to select data from one of said buffers to one of p of said p+k outputs of said input data conditioner.

8. (Original) The switch of claim 7, wherein said input data conditioner comprises k, p input, one output data selectors, for selecting from one of its p inputs data to be output at one of k of said p+k outputs of said input data conditioner.

9. (Original) The switch of claim 1, wherein said output data conditioner comprises k one input, p output switches, each for switching data from its input to one of its p outputs.

10. (Original) The switch of claim 9, wherein said output data formatting block comprises p k+1 input, 2(p+k) output switches for ordering data units received at said p+k inputs of said output data formatting block.

11. (Original) The switch of claim 10, wherein said output data formatting block comprises p sets of 2(p+k) intermediate buffers, each in communication with one of said p output switches.

12. (Original) The switch of claim 11, wherein said output data formatting block comprises p 2(p+k) input, one output data distributors, each for providing an output from said data conditioner from one set of said intermediate buffers.

13. (currently amended) A communications switch, comprising:

p inputs and q outputs;

a rotator switch comprising a (p+k)x(p-K) switch fabric;

an input data conditioner for distributing data received at said p inputs to said switch fabric;

an output data conditioner in communication with said switch fabric for distributing data received from said switch fabric to said q outputs;

wherein p, q, and k are positive integers.

14. (Original) The communication switch of claim 13, wherein p=q.

15. (Original) The communications switch of claim 14, wherein said rotator switch comprises p+k information storage buffers and wherein said switch fabric is clocked at a rate so as to switch less traffic through each of said p+k information buffers than arrives at one of said inputs in a clock cycle.

16. (Original) The communications switch of claim 15, wherein said rotator switch comprises p+k information storage buffers and wherein said switch fabric is clocked at a rate so as to transfer an amount of traffic through said p+k information buffers equaling at least an amount arriving at all of said p inputs in said clock cycle.

17. (currently amended) A method of switching data between p inputs and q outputs, comprising:

distributing data from said p inputs to p+k intermediate inputs;

loading data from said p+k inputs into p+k tandem buffers, each of said tandem buffers comprising p+k storage locations;

unloading one location of each of said p+k tandem buffers at one of p+k intermediate outputs;

combining data from said p+k intermediate outputs to provide switched data from said p inputs at said q outputs;

wherein p, q, and k are positive integers.

18. (Original) The method of claim 17, further comprising cyclically interconnecting said p+k tandem buffers with said p+k intermediate inputs and said p+k intermediate outputs.

19, (Original) The method of claim 18, wherein data is loaded into said tandem buffers at a rate lower than a rate of traffic arriving at each of said p inputs.

20. (Original) The method of claim 17 wherein data is loaded into all of said tandem buffers at a rate at least equal to a rate of arrival of data at all of said p inputs.

21. (Original) The method of claim 18, wherein said p+k tandem buffers are cyclically interconnected at a rate of 1/t to load data to each of said tandem buffers for data arriving at each of said inputs at a rate of 1/t', where t' = t*p/(p+k).

22. (Original) The method of claim 19, wherein at least some of said data is transferred to a selected location of an interconnected tandem buffer, said location based on a destination for said at least some of said data.

23. (Original) The method of claim 19, further comprising combining data into data units, and including a header in each of said data units, each header including destination information and a sequence number for said each of said data units.

24. (previously amended) The method of claim 23, wherein said combining further comprises stripping said headers from said data units.

25. (currently amended) A communications switch for switching information units between inputs and outputs, said switch comprising:

p inputs each for receiving data to be switched to q outputs;

p+k information storage buffers, each of said information storage buffers comprising p+k storage locations;

means for distributing data received at said p inputs to p+k intermediate inputs;

means for cyclically interconnecting each of said p+k intermediate inputs to one of said p+k information storage buffers;

means for distributing data from said p+k information storage buffers to said p outputs;

means for cyclically interconnecting each of said p+k information storage buffers to said means for distributing data from said p+k information storage buffers;

wherein p, q, and k are positive integers.